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## **DMA ACKNOWLEDGE SIGNAL FOR AN IDE DEVICE**

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### **BACKGROUND OF THE INVENTION**

5           The present invention relates to integrated drive electronics disc drive access and more particularly to direct memory access for integrated drive electronics type disc drives.

10           Integrated Drive Electronics (IDE) is a type of hardware interface widely used to connect hard disks, CD-ROMS and tape drives to a computer system. With an IDE type disc drive, drive controller electronics are built into the drive itself. In known computer systems, IDE drives are attached to a computer system using an IDE host adapter card. Alternately, one or more Enhanced IDE (EIDE) sockets may be built onto a computer system motherboard.; each socket may connects up to two IDE drives.

15           The IDE interface conforms to the AT Attachment (ATA) specification. A variation of the ATA specification is the ATA Packet Interface (ATAPI) which defines an IDE interface for CD-ROMs and tape drives. Another variation of the ATA specification is the Fast ATA (ATA-2) which defines faster transfer rates used in Enhanced IDE (EIDE). Another variation of the ATA specification is the ATA-3  
20           which adds interface improvements, including the ability to report potential problems.

          A known type of memory access is referred to as a Direct Memory Access (DMA). A DMA transfer transfers data directly from one memory to another memory without using a system processor. Although DMA may periodically steal cycles from a processor, data are transferred much faster than if a system processor were involved  
25           with every byte of the data transfer.

One challenge associated with systems providing an IDE interface to an IDE type drive relates to enabling DMA data transfers in systems in which DMA transfers are not enabled within the IDE interface.

### **SUMMARY OF THE INVENTION**

5           In accordance with the present invention, a system is provided with an IDE interface which includes a DMA acknowledge control circuit to enable DMA data transfers to an IDE type device.

10           In one embodiment, the invention relates to a method for using a personal computer memory card international association (PCMCIA) controller to communicate with an Integrated Drive Electronics (IDE) drive which includes performing a transfer between the static random access memory (SRAM) controller and the IDE drive using PCMCIA interface signals to communicate with the IDE drive and a general purpose input/output signal to communicate with an interrupt request of the IDE drive.

15           In another embodiment, the invention relates to a method for using a personal computer memory card international association (PCMCIA) controller to communicate with an Integrated Drive Electronics (IDE) drive which includes performing a transfer between the PCMCIA controller and the IDE drive using PCMCIA interface signals to communicate with the IDE drive, and generating a  
20   DMA acknowledge signal based upon a DMA request signal and a chip enable signal.

25           In another embodiment, the invention relates to an apparatus for communicating with an Integrated Drive Electronics (IDE) drive which includes a personal computer memory card international association (PCMCIA) controller, the PCMCIA controller interfacing with signals conforming to a PCMCIA interface, the PCMCIA controller performing a transfer between the PCMCIA controller and an IDE drive using the PCMCIA interface signals to communicate with the IDE drive, and a DMA acknowledge control circuit, the DMA acknowledge control circuit generating a DMA acknowledge signal based upon a DMA request signal and a chip enable signal.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention may be better understood, and its numerous objects, features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference number throughout the  
 5 several figures designates a like or similar element.

Figure 1 shows a schematic block diagram of a system which includes a DMA acknowledge control circuit.

Figure 2 shows a diagram of the signal connections between processor signals and IDE drive signals.

10 Figure 3 shows a schematic block diagram of a DMA acknowledge control circuit.

Figure 4 shows a truth table of the operation of the DMA acknowledge control circuit.

## **DETAILED DESCRIPTION**

Referring to figure 1, system 100 designed for use in mobile information appliances. System 100 is preferably a complete system on a chip (SOC) based on a MIPS32 instruction set. The system 100 is designed to operate at low power.

20 System 100 includes a processor 110, a synchronous dynamic random access memory (SDRAM) controller 112, a static random access memory (SRAM) controller 114, a real time clock 116, a power management module 118 and a peripheral device control module 120 all interconnected via bus 130.

The peripheral device control module 120 may be coupled to one or more peripheral devices such as an Ethernet multiply-Accumulate (MAC) controller, a  
 25 universal serial bus (USB) device and host controller, a universal asynchronous

receiver transmitter (UART) controller, an Infrared Data Association (IrDA) controller, an audio code '97 (AC'97) controller, and a secure digital (SD) controller.

SDRAM controller 112 is coupled to SDRAM 140. SRAM controller 114 is coupled to a static bus 150. The static bus 150 is a general purpose bus which  
5 includes a 32-bit address path, a 32-bit data bus, a plurality of control signal paths, including a plurality of general purpose I/O signal paths. Some or all of the control signal paths and the general purpose I/O signal paths may be used depending on the type of device with which the SDRAM controller 114 is communicating.

Static bus 150 is also coupled to one or more static bus devices such as, e.g.,  
10 an LCD controller 160, a personal computer memory card international association (PCMCIA) device 162, a flash memory device 164, SRAM 166, read only memory (ROM) 168 and an expansion bus 170. Static bus 150 is also coupled to a DMA acknowledge control circuit 180. The DMA acknowledge control circuit 180 is in turn coupled to an IDE connector 182 to which an IDE disk drive 183 may be  
15 connected. The SRAM controller 114 functions as a general purpose bus controller and may communicate with any one of a plurality of static bus devices. For example, when SRAM controller 114 is communicating with the SRAM 166, then SRAM controller 114 functions as an SRAM controller. When SRAM controller 114 is communicating with a PCMCIA device 162, then the SRAM controller 114 functions  
20 as a PCMCIA controller.

The static bus 150 may interface with Integrated Drive Electronics (IDE) hard drives via a modified PCMCIA interface. Such an interface eliminates the need for an external disk drive controller. The static bus 150 interfaces with IDE drives via the DMA acknowledge control circuit 180. The DMA acknowledge control circuit 180  
25 provides a direct interface with an IDE drive when accessing the IDE drive in PIO mode. The DMA acknowledge control circuit 180 enables a circuit which is not designed for DMA access to IDE to perform a DMA data transfer to IDE. The DMA transfer mode is a master transfer mode. The DMA transfer is initiated by the processor 110. When communicating with the IDE drive in a PIO mode, the interface  
30 is directly between the SRAM controller 114 and the IDE drive 183; there is no need for the DMA acknowledge signal to be generated.

Referring to Figure 2, one of the modes in which the SRAM controller 114 functions is as a PCMCIA interface in which the SRAM controller 114 provides a PCMCIA interface. The PCMCIA interface may be used by the SRAM controller 114 to provide an IDE interface. More specifically, when the SRAM controller 114 is configured for the PCMCIA mode, as indicted via the static bus chip select signal, the signals set forth in Figure 2 are used to interface to an IDE device via the IDE connector 182.

More specifically, when providing an IDE interface, certain PCMCIA interface signals correspond to certain IDE interface signals. For example, the PCMCIA reset signal ( $\overline{RESET\_OUT}$ ), which is used reset a PCMCIA device, corresponds to the IDE reset signal ( $\overline{RESET}$ ), which is used to reset the IDE disk drive. The 3-bits of the PCMCIA address bus (RAD[2:0]), correspond to three bits of the IDE address bus (DA[2:0]), which correspond to bits 2 – 0 of the address bus of the IDE interface. The 16 bits of the PCMCIA data bus (RD[15:0]) are bi-directionally coupled with the 16 bits DD[15:0] signal, which correspond to bits 15 – 0 of the data bus of the IDE interface. The PCMCIA write cycle indication ( $\overline{PIOW}$ ), which is an output signal indicating an I/O write cycle, corresponds to the IDE write signal ( $\overline{DIOW}$ ), which indicates to the IDE disk drive to write data over the I/O channel. The PCMCIA read cycle indication ( $\overline{PIOR}$ ), which is an output signal indicating an I/O read cycle, corresponds to the IDE read signal ( $\overline{DIOR}$ ), which indicates to the IDE disk drive to read data over the I/O channel.

Bit zero of the 2-bit PCMCIA enable ( $\overline{PCE[0]}$ ), which are active low card enable bits, correspond to the IDE chip select signal (CS1Fx(master)), which indicates a chip select for base address 1f0h. The processor signal  $\overline{PCE[0]}$  functions as a chip select for the IDE drive.

The n bit of the GPIO signal, GPIO[n], which is a general purpose I/O signal of the static bus 150, receives the INTRQ signal, which indicates an interrupt request from the IDE drive. The GPIO[n] signal functions as an interrupt from the IDE drive

to the processor 110. The IDE interrupt may be coupled to any available GPIO signal path of the static bus 150.

Additionally, the PCMCIA port select signal ( $\overline{PIOS16}$ ) is pulled down (i.e., is active) to indicate that the IDE drive operates in a 16-bit mode (this signal may be connected directly to the IDE drive via the connector 182). The PCMCIA wait signal ( $\overline{PWAIT}$ ) is pulled up to indicate not to delay completion of a pending cycle.

Additionally, a plurality of PCMCIA signals are not needed or used for the IDE disk drive. For example, the PCMCIA output enable signal ( $\overline{ROE}$ ) is not connected, Bit 1 of the two bit PCMCIA chip enable signal ( $\overline{PCE[1]}$ ) is not connected, the PCMCIA memory output enable signal ( $\overline{POE}$ ) is not connected, the PCMCIA memory write enable signal ( $\overline{PWE}$ ) is not connected, and the attribute memory access signal ( $\overline{PREG}$ ) is not connected.

When functioning in a DMA access mode, SRAM controller 114 in conjunction with the DMA acknowledge control circuit 180 generate and use additional signals. More specifically, the GPIO[4] signal functions as a DMA request signal from the IDE drive. The GPIO[5] signal could also be used for this function. GPIO[n] is an interrupt from the IDE drive to the processor (the IDE interrupt can be tied to any available GPIO).

The DMA acknowledge control circuit 180 generates the IDE DMA acknowledge signal (DMACK) based upon a combination of the chip enable signal  $\overline{PCE[0]}$  and the DMA request signal (DMARQ).

Referring to Figure 3, the DMA acknowledge control module 180 generates a DMA acknowledge (DMACK) signal to the IDE drive via the DMA request from the IDE drive and the  $\overline{PCE[0]}$  signal from the processor 110. This assumes a zero delay from DMA request to DMA acknowledge for the IDE specification. The  $\overline{PCE[0]}$  signal is used to ensure the hold time after the last transfer.



The DMA acknowledge control module 180 includes OR gate 310, AND gate 320 and inverter 330. Inverter 330 receives the DMA request signal (DMARQ) signal and generates an inverted DMARQ signal. OR gate 310 receives a chip enable ( $\overline{PCE[0]}$ ) signal as well as the DMACK signal.

5           Figure 4 sets forth the operation of the DMA acknowledge control module 180. More specifically, when  $DMARQ = 1$ ,  $\overline{DMACK} = 0$ . The state of the  $\overline{PCE[0]}$  signal has no affect on the  $\overline{DMACK}$  signal. When  $DMARQ = 0$  and  $\overline{PCE[0]} = 1$ ,  $\overline{DMACK} = 1$ . When  $DMARQ = 0$  and  $\overline{PCE[0]} = 0$ ,  $\overline{DMACK} = \overline{DMACK}$ . I.e.,  $\overline{DMACK}$  does not change.

10           When generating a DMA request, the processor 110 is configured to use one of the external DMA request lines: DMA\_REQ0 (GPIO4) or DMA\_REQ1 (GPIO5). The processor 110 may also use GPIO208 and GPIO209.

          The DMA is configured in the DMA\_modeset register for a Device Address High (DAH) value of 1111 (for the upper address bits for PCMCIA), Device ID  
15 (DID) of 2 for DMA\_REQ0, transfer size (TS) of 4, and device width (DW) of 16 bits.

          In operation, the processor 110 initializes the DMA channel to use an external request. The processor 110 writes the command to the IDE drive 183. The IDE drive sets the busy BSY bit. When the drive is ready for a transfer, the drive sets the  
20 DMARQ signal. The processor 110 detects that the DMARQ is set and transfers the data. When all of the data has been transferred, the IDE drive 183 asserts the interrupt request signal INTRQ signal. When the processor 110 detects the INTRQ signal, the processor reads the STATUS register of the IDE drive 183. The IDE drive 183 clears the INTRQ signal when the STATUS register is read by the processor 110.

25           The present invention is well adapted to attain the advantages mentioned as well as others inherent therein. While the present invention has been depicted, described, and is defined by reference to particular embodiments of the invention, such references do not imply a limitation on the invention, and no such limitation is to be inferred. The invention is capable of considerable modification, alteration, and

equivalents in form and function, as will occur to those ordinarily skilled in the pertinent arts. The depicted and described embodiments are examples only, and are not exhaustive of the scope of the invention.

5 For example, while the DMA acknowledge control circuit is shown with a particular configuration of logic, it will be appreciated that other logic configurations may be used to achieve functionally equivalent results.

Also for example, while the DMA acknowledge control circuit is shown as a discrete circuit, it will be appreciated that such a circuit could be incorporated into either the SRAM controller or the IDE interface.

10 Also, for example, while certain portions of the preferred embodiment are shown as active low and other portions as active high, it will be appreciated that the choice of whether a signal, a circuit or portion thereof is active low or active high is merely one of design.

Also, for example, the above-discussed embodiments include modules that  
15 perform certain tasks. The modules discussed herein may include be instantiated as hardware, software or some combination of hardware and software. Additionally, those skilled in the art will recognize that the separation of functionality into modules is for illustrative purposes. Alternative embodiments may merge the functionality of multiple modules into a single module or may impose an alternate decomposition of  
20 functionality of modules.

Consequently, the invention is intended to be limited only by the spirit and scope of the appended claims, giving full cognizance to equivalents in all respects.